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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,379	01/21/2004	Sean G. Gibb	PAT 943-2	2143

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EXAMINER	
DO, CHAT C	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/760,379	Applicant(s) GIBB ET AL.	
	Examiner Chat C. Do	Art Unit 2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/24/04; 05/25/04; 12/07/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/25/04;12/07/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The applicant is advised to update information cite under the "Cross-Reference to Related Applications" in page 1 of the original specification.

In addition, there is a limitation cited in page 24 in lines 8-9 without any claimed No.

Appropriate correction is required.

Claim Objections

2. Claims 1, 8, 15, and 20 are objected to because of the following informalities:

Re claim 1, the applicant is advised to rewrite the term "co-efficient" as "coefficient" as seen in lines 3-4.

Re claim 8, the applicant is advised to rewrite the term "N2" in line 2 as "N/2".

Re claim 15, it has the same objection as cited in claim 1 above.

Re claim 20, the applicant is advised to rewrite the term "modulehaving" as "module having" in line 6.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-24 cite a FFT processor for transforming an input sequence according to a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or concrete, useful, and tangible result. However, claims 1-24 are merely discloses steps and components for performing Fast Fourier Transform in hardware without disclosing a practical application or a tangible final result. Therefore, claims 1-24 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeh (U.S. 2004/0059766).

Re claim 1, Yeh discloses in Figures 1-16 a pipelined fast Fourier transform (FFT) processor for receiving an input sequence (e.g. Figure 3 and abstract wherein the input sequence is x(k) and paragraph [0008]), the processor comprising: at least one FFT

triplet (e.g. Figure 3 part 37 is the triplet FFT module) having first, second and third butterfly modules connected in series (e.g. 31a, 32, and 33 modules respectively in Figure 3) by selectable multipliers for selectively performing trivial co-efficient multiplication and complex co-efficient multiplication on output sequences of adjacent butterfly modules (e.g. controlling by 36 and its complex coefficients 36b in Figure 3), each of the at least one FFT triplets terminating in a twiddle factor multiplier for applying a twiddle factor to an output of the third butterfly module of the respective triplet (e.g. see Figure 9 with twiddle factor multipliers as Wx), the at least one FFT triplet for receiving the input sequence and for outputting a final output sequence representing an FFT of the input sequence (e.g. the last stage of computation as seen in Figure 9 with BFII as the last stage of 32 input sequence).

Re claim 2, Yeh further discloses in Figures 1-16 each butterfly module includes a radix-2 butterfly unit and a feedback memory (e.g. Figure 3 with 37 as triplet module wherein the module consists of three separate sub-modules wherein each sub-module consists of a butterfly operation and its feedback memory).

Re claim 3, Yeh further discloses in Figures 1-16 for an input sequence of N samples, an output sequence X(k, n) of each butterfly module is equal to 20 x (n) + (- 1) k x (n + N/2) (e.g. inverse processed in BFII of Figure 9).

Re claim 4, Yeh further discloses in Figures 1-16 at least one of the selectable multipliers for performing trivial co-efficient multiplication is integrated in an adjacent butterfly module (e.g. Figure 10 with 608).

Re claim 5, Yeh further discloses in Figures 1-16 the selectable multipliers each include a multiplier and a switch for bypassing the multiplier (e.g. by the control unit in Figure 10 with Figure 14).

Re claim 6, Yeh further discloses in Figures 1-16 the first and second butterfly modules are connected by a selectable multiplier for selectively applying trivial co-efficient multiplication (e.g. Figure 11B with j multiplication in BFII).

Re claim 7, Yeh further discloses in Figures 1-16 the second and third butterfly modules are connected by a selectable multiplier for performing trivial co-efficient multiplication and a selectable multiplier for performing the complex co-efficient multiplication W.sub.N.sup.N/8 (e.g. Figure 11B with jW and W multiplication in BFIII).

Re claim 8, Yeh further discloses in Figures 1-16 for an input sequence having N samples, the feedback memories for the first, second and third butterfly modules hold N/2, N/4 and N/8 samples, respectively (e.g. Figure 3 with part 37 wherein each feedback memory holds appropriated size of input data).

Re claim 9, Yeh further discloses in Figures 1-16 the input sequence is of length N, where (log.sub.2N)mod3=1, the processor having a plurality of FFT triplets in seriatim and further including an FFT terminator having a butterfly unit and a corresponding memory sized to hold a single sample, the FFT terminator for receiving the output sequence from the final twiddle factor multiplier and for performing a butterfly operation on the received output sequence to render an FFT of the input sequence (e.g. as the case of Figure 3).

Re claim 10, Yeh further discloses in Figures 1-16 the input sequence is of length N, where (log.sub.2N)mod3=2, the processor having a plurality of FFT triplets in seriatim and further including an FFT terminator having first and second butterfly units having corresponding memories sized to hold two samples and a single sample respectively, the first butterfly unit connected to the second butterfly unit by a selectable multiplier for selectively multiplying the output of the first butterfly unit by -j, the FFT terminator for receiving the output sequence from the final twiddle factor multiplier and for performing a pair of butterfly operations on the received output sequence to render an FFT of the input sequence (e.g. as the case of Figure 10 and its corresponding Figure 11A).

Re claim 11, Yeh further discloses in Figures 1-16 the twiddle factor multiplier is a cordic rotator (e.g. 208 in Figure 5).

Re claim 12, Yeh discloses in Figures 1-16 a pipelined fast Fourier transform (FFT) processor for receiving an input sequence of N samples (e.g. abstract and Figure 3 wherein the input is either x(n)/X(N) depending on the processed of FFT/IFFT respectively), the processor comprising: at least one FFT triplet (e.g. part 37 in Figure 3), the triplet having: a first FFT stage having a first stage radix-2 butterfly unit for receiving the input sequence and for providing a first stage output sequence in accordance with a butterfly operation performed on the input sequence (e.g. 31a and 8 in Figure 3), the first stage radix-2 butterfly unit having a first feedback memory connected thereto; a second FFT stage having a selectable multiplier for selectively multiplying the first stage output

sequence by a trivial co-efficient, and a second stage radix-2 butterfly unit for providing a second stage output sequence in accordance with the butterfly operation performed on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto (e.g. part 32 and 4 in Figure 3); and a third FFT stage having a multiply selectable multiplier for selectively multiplying the second stage output sequence by at least one of the trivial co-efficient and a complex co-efficient, a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the multiply selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output sequence corresponding to an FFT of the input sequence (e.g. part 33 and 2 in Figure 3) (e.g. wherein each of the stage of BF is clearly addressed or shown in Figures 4-6 respectively).

Re claim 13, Yeh further discloses in Figures 1-16 each of the first, second and third stage output sequences X(k,n) is equal to 21 x (n) + (- 1) k x (n + N/2) (e.g. inverse processed in BFII of Figure 9).

Re claim 14, Yeh further discloses in Figures 1-16 at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial co-efficient multiplication to a received input sequence (e.g. Figure 9 with BFII and BFIII).

The FFT processor of claim 12, further including an FFT terminator determined in accordance with the length N of the input sequence (e.g. either Figure 3 or Figure 10).

Re claim 15, Yeh discloses in Figures 1-16 a pipelined fast Fourier transform (FFT) processor for receiving an input sequence of N samples (e.g. triplet 37 in Figure 3 and the abstract wherein the input sequence is either x(n)/X(N) depending on the processed FFT/IFFT respectively), the processor comprising: at least one FFT triplet (e.g. triplet 37 in Figure 3), the triplet having: a first FFT stage having a first stage radix-2 butterfly unit for receiving the input sequence and for providing a first stage output sequence in accordance with a butterfly operation performed on the input sequence, the first stage radix-2 butterfly unit having a first feedback memory connected thereto (e.g. BFI 31a and 8 in Figure 3); a second FFT stage having a multiply selectable multiplier for selectively multiplying the first stage output sequence by at least one of the trivial co-efficient and a constant complex co-efficient, and a second stage radix-2 butterfly unit for providing a second stage output sequence in accordance with the butterfly operation performed on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto (e.g. BFII 32 and 4 in Figure 3); and a third FFT stage having a selectable multiplier for selectively multiplying the second stage output sequence by a trivial co-efficient, a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output sequence corresponding to an FFT of the input sequence (e.g. part 33 and 2 in Figure 3) (e.g. wherein each of the stage of BF is clearly addressed or shown in Figures 4-6 respectively).

Re claim 16, Yeh further discloses in Figures 1-16 each of the first, second and third stage output sequences X(k,n) is equal to 22 x (n) + (- 1) k x (n + N/2) (e.g. inverse processed in BFII of Figure 9).

Re claim 17, Yeh further discloses in Figures 1-16 at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial co-efficient multiplication to a received input sequence (e.g. Figure 9 with BFII and BFIII).

Re claim 18, Yeh further discloses in Figures 1-16 an FFT terminator determined in accordance with the length N of the input sequence (e.g. either Figure 3 or Figure 10).

Re claim 19, Yeh further discloses in Figures 1-16 the FFT terminator includes a butterfly module having a memory sized to store a single sample, for receiving as a terminator input, the output of the third FFT stage multiplier and for performing a butterfly operation on the terminator input to render an FFT of the input sequence of N samples (e.g. as with the BFI as seen in Figure 3).

Re claim 20, Yeh further discloses in Figures 1-16 the FFT terminator includes a first butterfly module having a memory sized to store a pair of samples, for receiving as a terminator input, the output of the third stage multiplier and for performing a butterfly operation on the terminator input, and a second butterfly module connected to the first butterfly module of the terminator by a selectable multiplier, the selectable multiplier for selectively multiplying the output of the first butterfly module of the terminator by -j, the second butterfly module having a memory sized to store a single sample and for performing a butterfly operation on the selectively multiplied output of the first butterfly

module of the terminator to render an FFT of the output sequence (e.g. as with the BFI and BFII as seen in Figure 10 and its corresponding Figure 11A).

Re claim 21, Yeh discloses in Figures 1-16 Yeh discloses in Figures 1-16 a method of performing an FFT on a sequence of N samples in an FFT processor having a butterfly module (e.g. Figure 3 and abstract), the method (e.g. for purposes of illustration Figures 2-3 are used to illustrate the features of prior art) comprising: for all integers 1.ltoreq.x.ltoreq.log.sub.2N (e.g. there are 16 input data label as X[0] to X[15]), repeating the steps of receiving and buffering 23 N 2 x samples at a time from a sequence having N samples (e.g. sampling and initialization); generating a 2-point FFT using the n.sup.th and the 24 (n + N 2 x) the samples (e.g. X[0] and X[8] are computed together); selectively multiplying the generated 2-point FFT sequence by a complex valued multiplicand (e.g. as seen in Figure 2 only the last four data are multiplied with j); terminating the FFT using a termination sequence determined in accordance with a (log.sub.2N)mod3 relationship (e.g. Figure 3 or Figure 10).

Re claim 22, Yeh further discloses in Figures 1-16 the complex valued multiplicand is selected from a list including 1, - j , sqrt(2)/2 - jsqrt(2)/2 ,and a complex twiddle factor co-efficient (e.g. Figures 3-6).

Re claim 23, Yeh further discloses in Figures 1-16 (log.sub.2N)mod3=1 and the step of terminating the FFT includes buffering a sample received from the final selective multiplication and performing a 2-point FFT using the buffered sample and the

subsequent sample in the sequence to obtain the FFT of the sequence of N samples (e.g. as with the BFI as seen in Figure 3).

Re claim 24, Yeh further discloses in Figures 1-16 (log.sub.2N)mod3=2 and the step of terminating the FFT includes: buffering a pair of samples received from the final selective multiplication and performing pair-wise 2-point FFTs using the two buffered samples and the two subsequent samples in the sequence; selectively multiplying the result of the pair-wise 2 point FFT by -j; and buffering a sample received from the selective multiplication of the pair-wise 2-point FFT and performing a 2-point FFT using the buffered sample and the subsequent sample in the sequence to obtain the FFT of the sequence of N samples (e.g. as with the BFI and BFII as seen in Figure 10 and its corresponding Figure 11A).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 4,821,224 to Liu et al. disclose a method and apparatus for processing multi-dimensional data to obtain a Fourier transform.

b. U.S. Patent No. 6,061,705 to Hellberg discloses a power and area efficient fast Fourier transform processor.

c. U.S. Patent No. 6,564,236 to Cambonie et al. disclose a device and associated method for calculating the direct or inverse Fourier Transform of the product of a complex symbol times a complex sinusoidal waveform.

d. U.S. Patent Publication No. 2002/0194235 to Yamamoto et al. disclose a processing apparatus.

e. U.S. Patent Publication No. 2004/00644493 to Kulkarni et al. disclose a reconfigurable vector-FFT/IFFT, vector-multiplier/divider.

f. U.S. Non-Patent Literature to Hasan et al. disclose an implementation of low-power FFT processor cores using a novel order-based processing scheme.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

February 1, 2007